FIG. 1

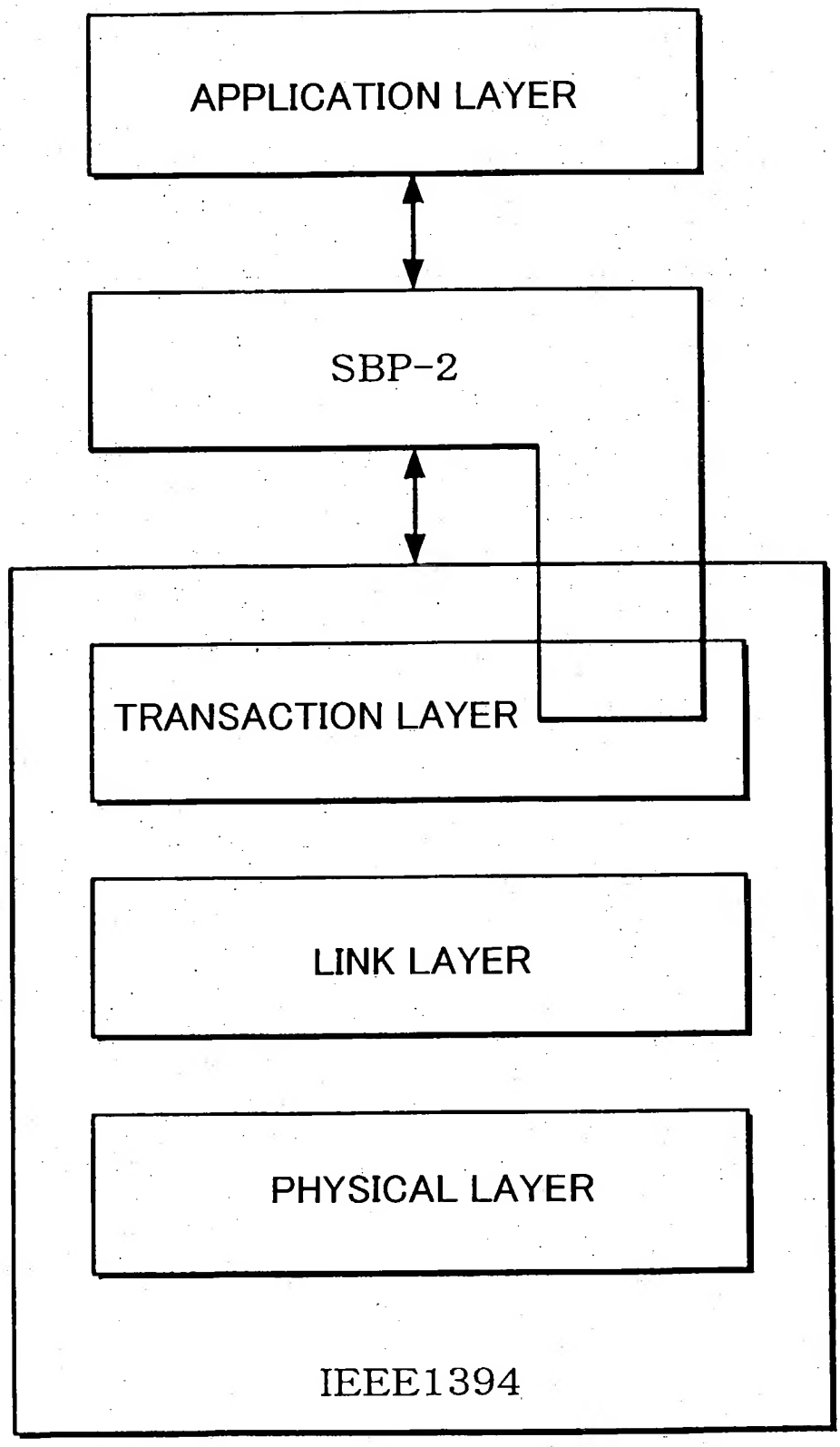
APPLICATION LAYER
SBP-2
TRANSACTION LAYER
LINK LAYER
PHYSICAL LAYER
IEEE1394

FIG. 2

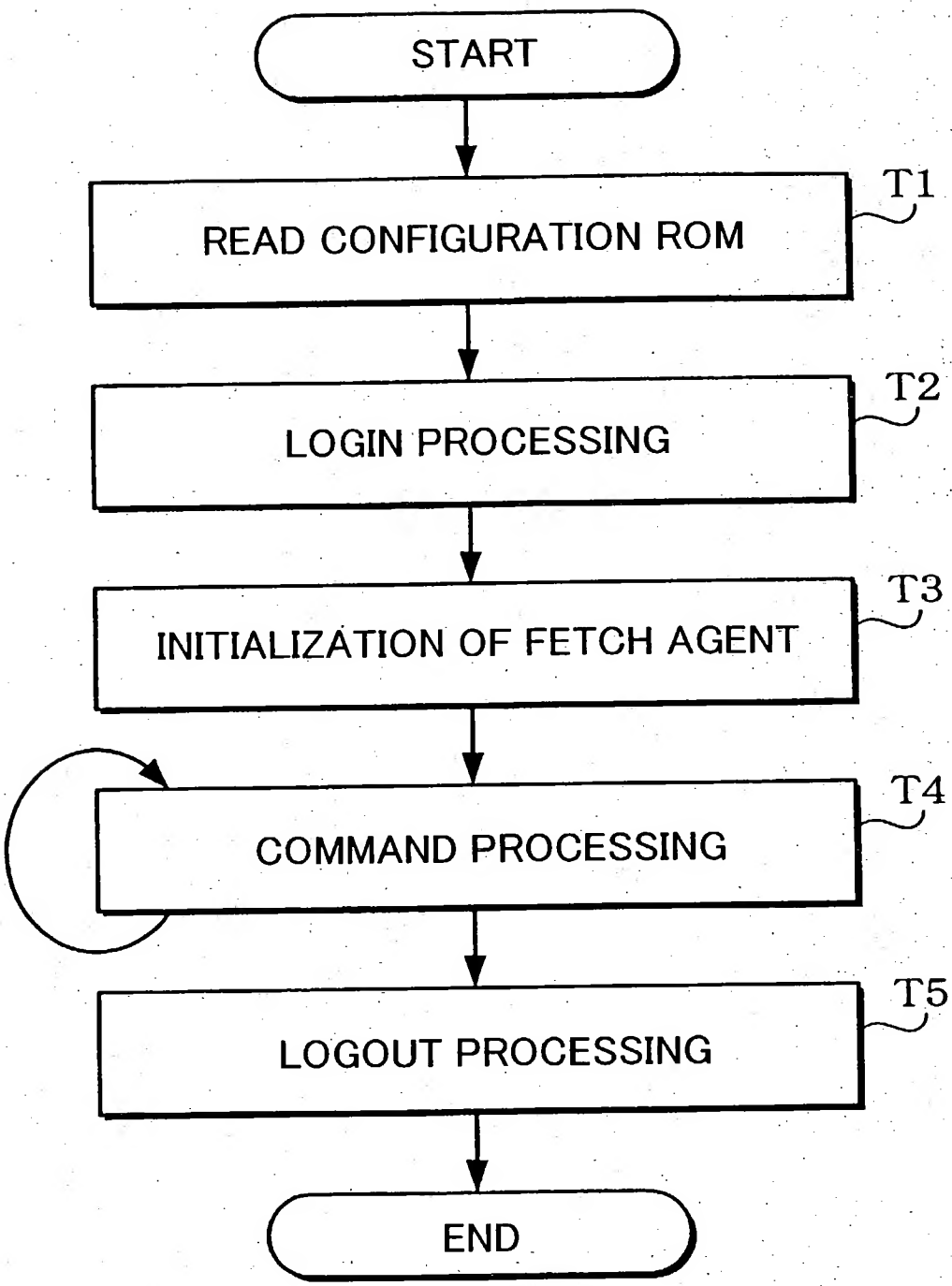
START
READ CONFIGURATION ROM
T1
LOGIN PROCESSING
T2
INITIALIZATION OF FETCH AGENT
T3
COMMAND PROCESSING
T4
LOGOUT PROCESSING
T5
END

FIG. 3

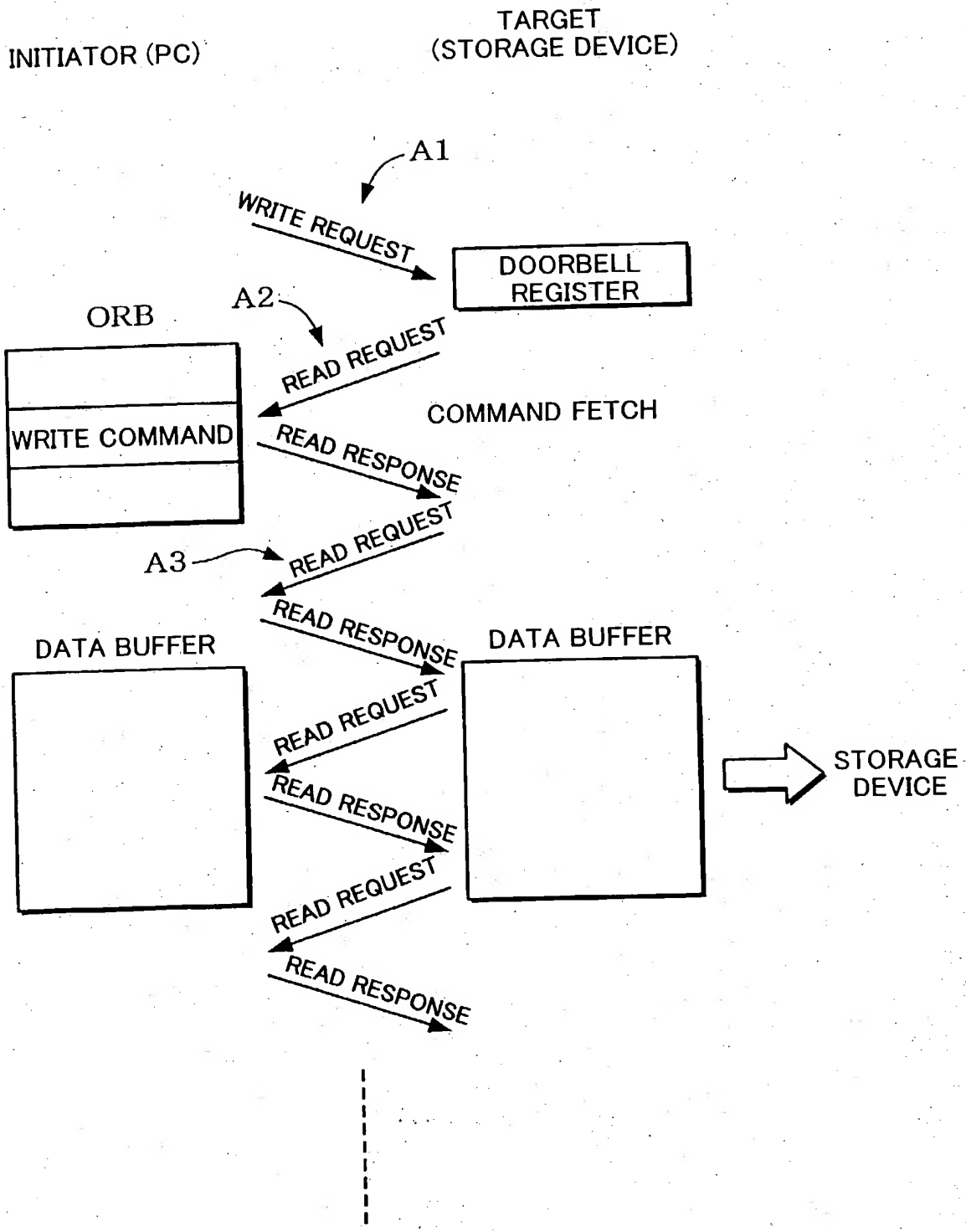
INITIATOR (PC)
TARGET
(STORAGE DEVICE)
A1
WRITE REQUEST
DOORBELL REGISTER
ORB
A2
READ REQUEST
WRITE COMMAND
COMMAND FETCH
READ RESPONSE
A3
READ REQUEST
READ RESPONSE
DATA BUFFER
DATA BUFFER
READ REQUEST
READ RESPONSE
STORAGE DEVICE
READ REQUEST
READ RESPONSE

FIG. 4

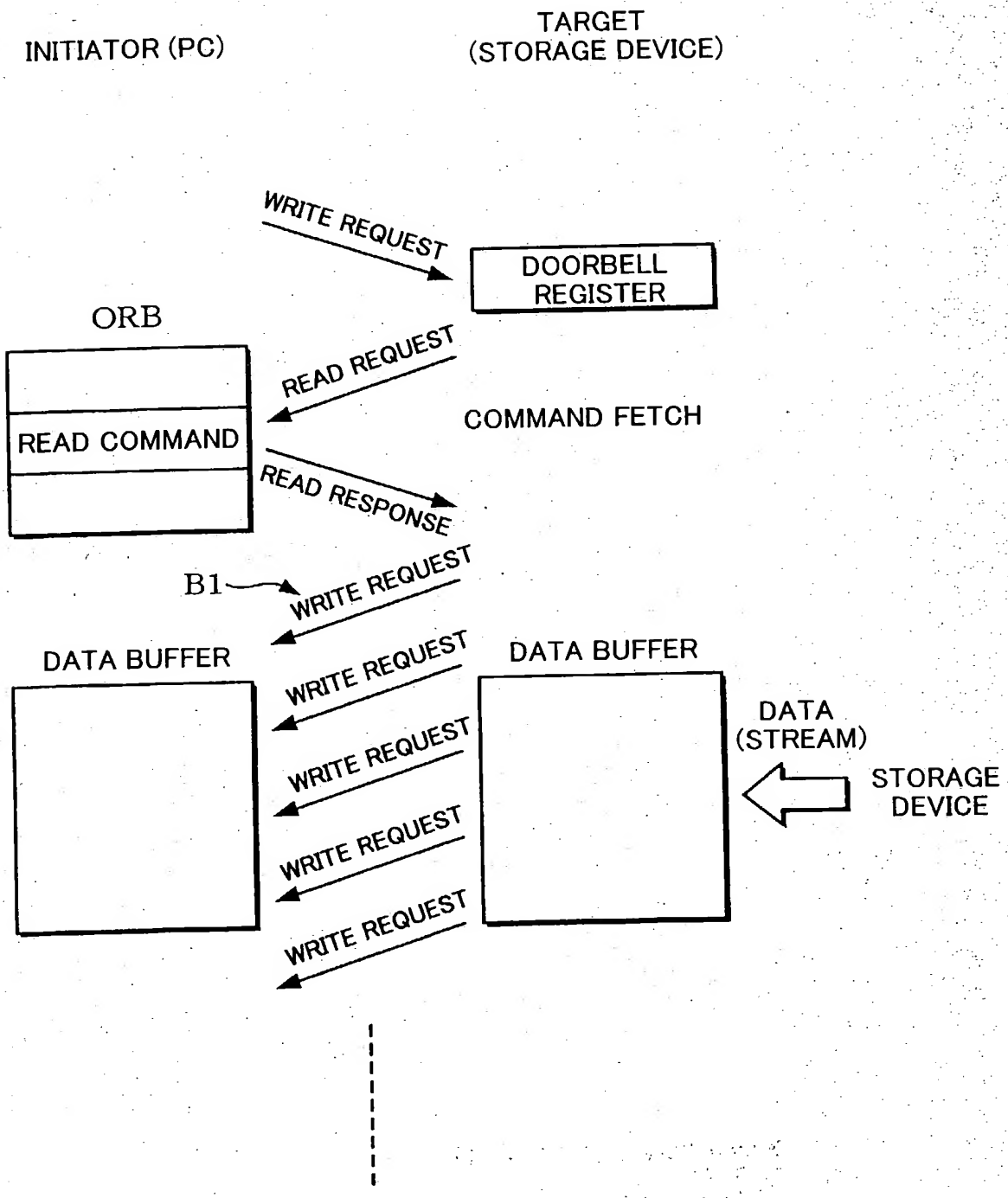
INITIATOR (PC)
TARGET
(STORAGE DEVICE)
WRITE REQUEST
DOORBELL
REGISTER
ORB
READ REQUEST
READ COMMAND
COMMAND FETCH
READ RESPONSE
B1
WRITE REQUEST
DATA BUFFER
WRITE REQUEST
DATA BUFFER
DATA
(STREAM)
WRITE REQUEST
STORAGE
DEVICE
WRITE REQUEST
WRITE REQUEST

FIG. 5A

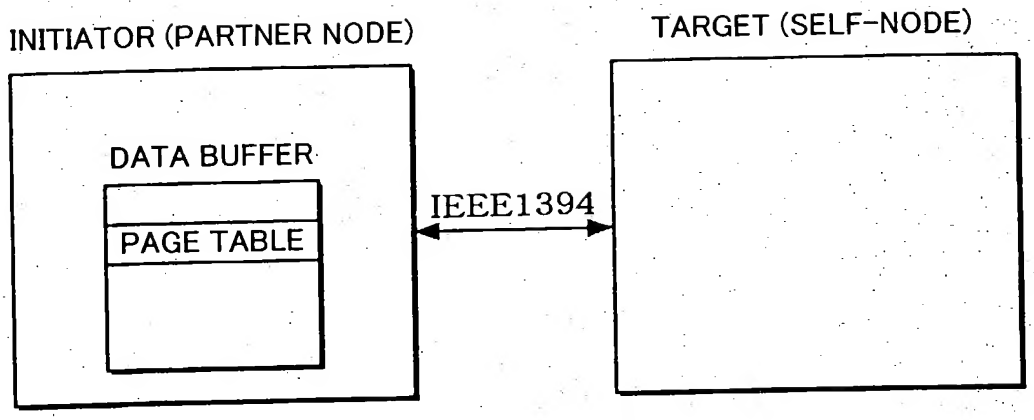

FIG. 5B PAGE TABLE IS PRESENT

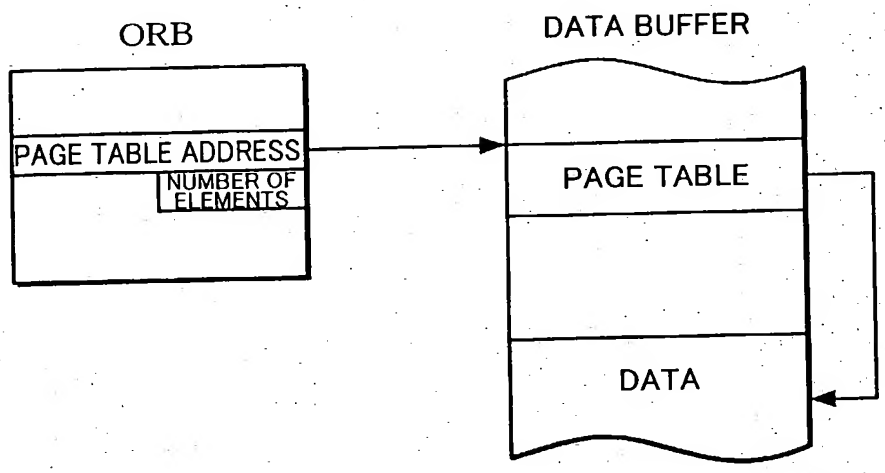

FIG. 5C PAGE TABLE IS NOT PRESENT

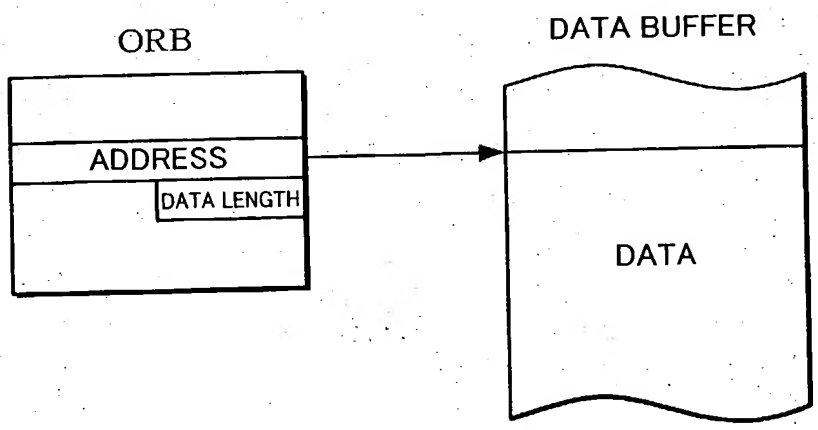

FIG. 6

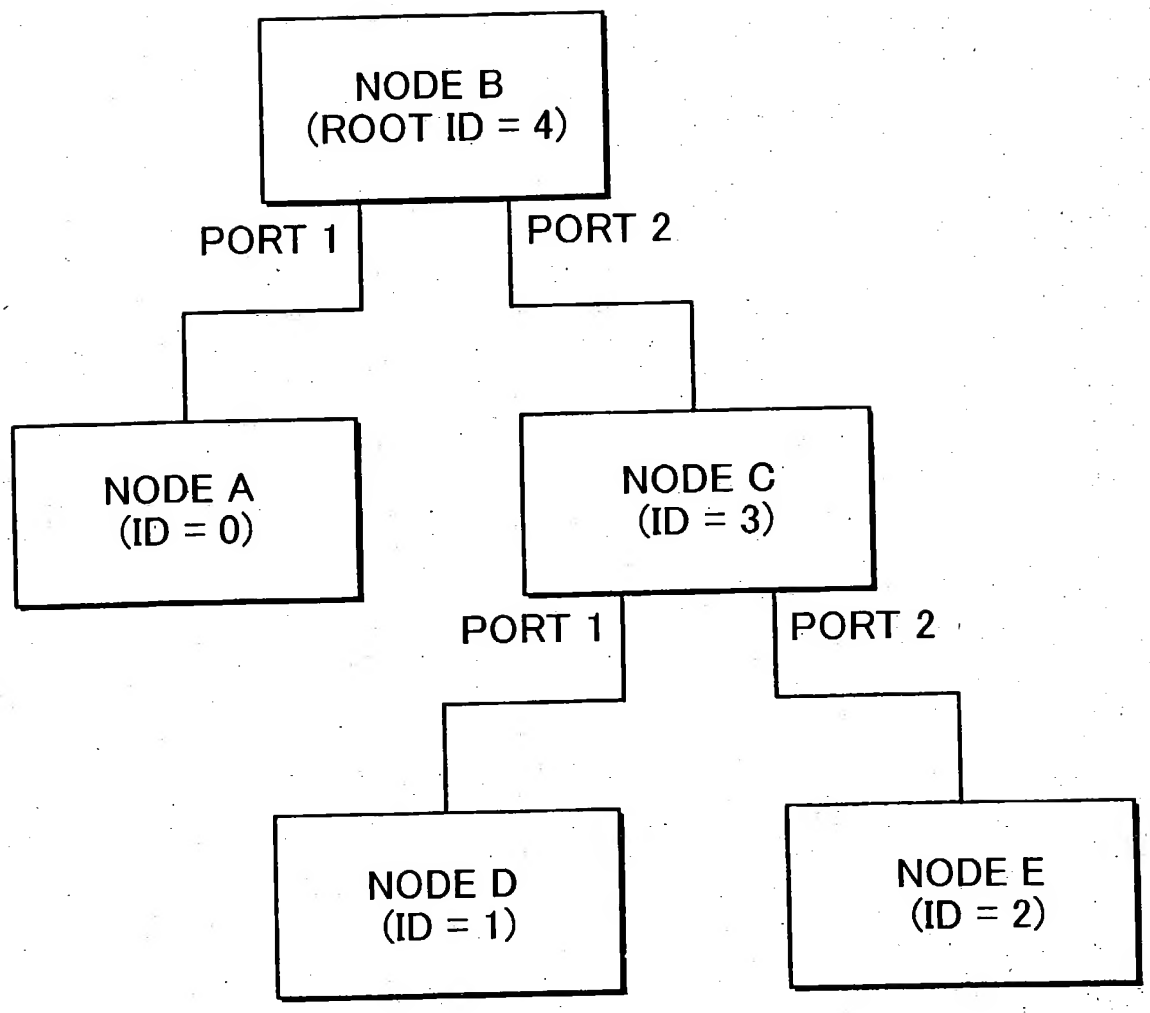
NODE B
(ROOT ID = 4)
PORT 1
PORT 2
NODE A
(ID = 0)
NODE C
(ID = 3)
PORT 1
PORT 2
NODE D
(ID = 1)
NODE E
(ID = 2)

FIG. 7A

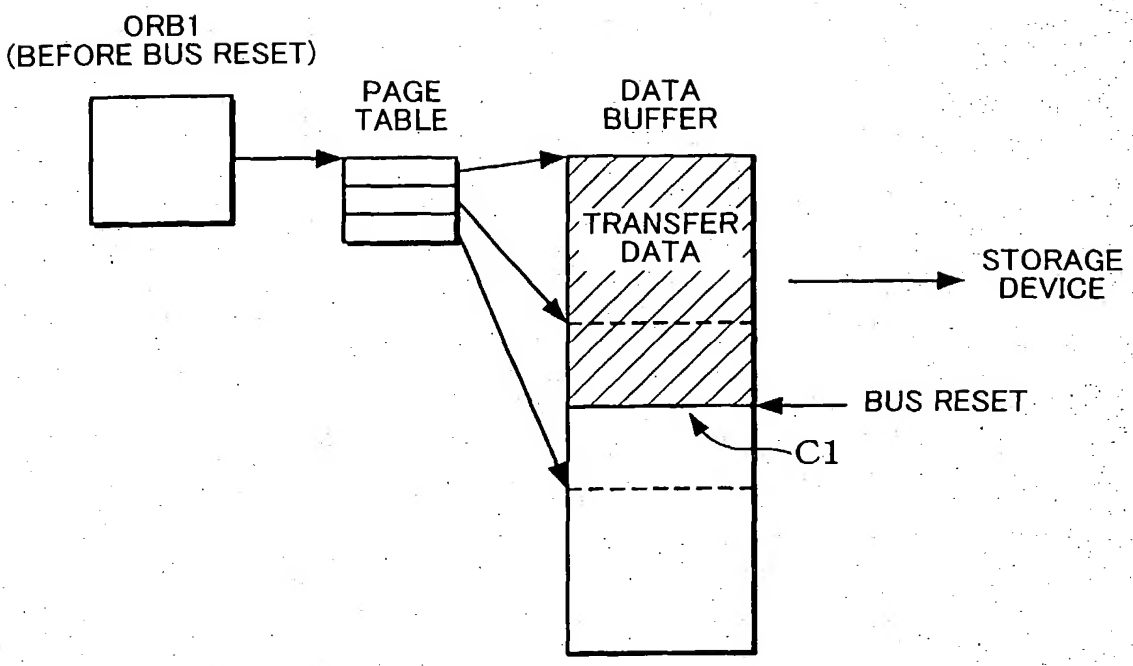
ORB1
(BEFORE BUS RESET)
PAGE TABLE
DATA BUFFER
TRANSFER DATA
STORAGE DEVICE
BUS RESET
C1

FIG. 7B

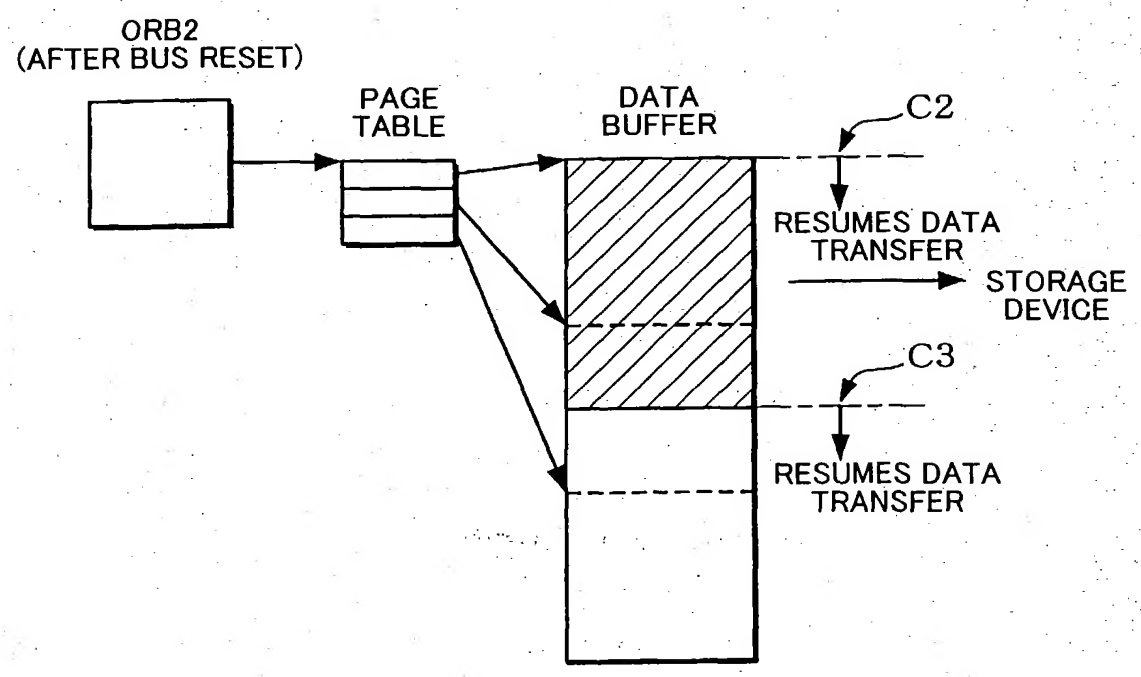
ORB2
(AFTER BUS RESET)
PAGE TABLE
DATA BUFFER
C2
RESUMES DATA TRANSFER
STORAGE DEVICE
C3
RESUMES DATA TRANSFER

FIG. 8

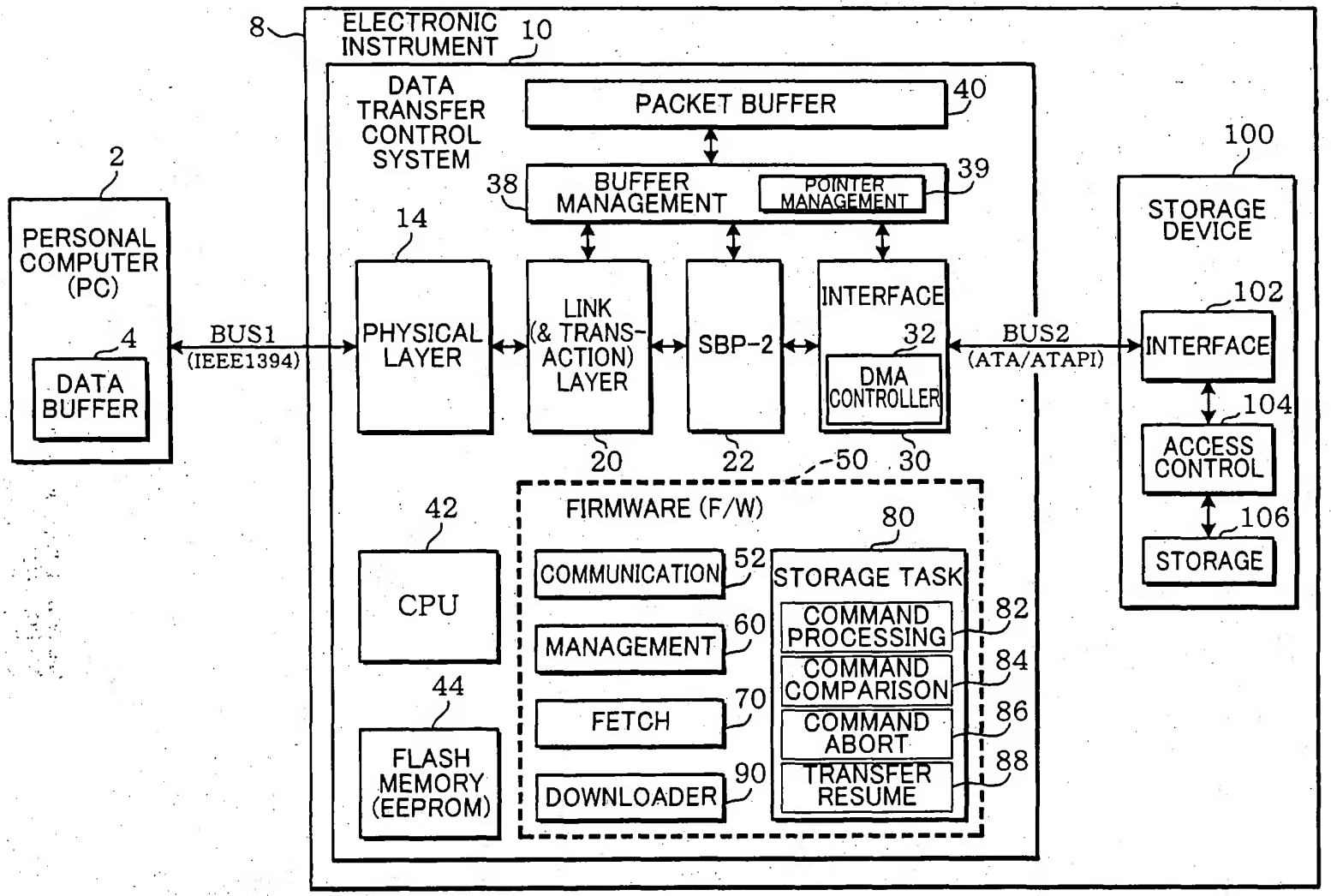
8
ELECTRONIC INSTRUMENT
10
DATA TRANSFER CONTROL SYSTEM
PACKET BUFFER
40
BUFFER MANAGEMENT
38
POINTER MANAGEMENT
39
2
PERSONAL COMPUTER (PC)
4
DATA BUFFER
BUS1 (IEEE1394)
14
PHYSICAL LAYER
LINK (& TRANS-ACTION) LAYER
SBP-2
INTERFACE
32
DMA CONTROLLER
20
22
50
30
BUS2 (ATA/ATAPI)
100
STORAGE DEVICE
102
INTERFACE
104
ACCESS CONTROL
106
STORAGE
42
CPU
44
FLASH MEMORY (EEPROM)
FIRMWARE (F/W)
80
COMMUNICATION
52
STORAGE TASK
MANAGEMENT
60
COMMAND PROCESSING
82
COMMAND COMPARISON
84
FETCH
70
COMMAND ABORT
86
DOWNLOADER
90
TRANSFER RESUME
88

FIG. 9

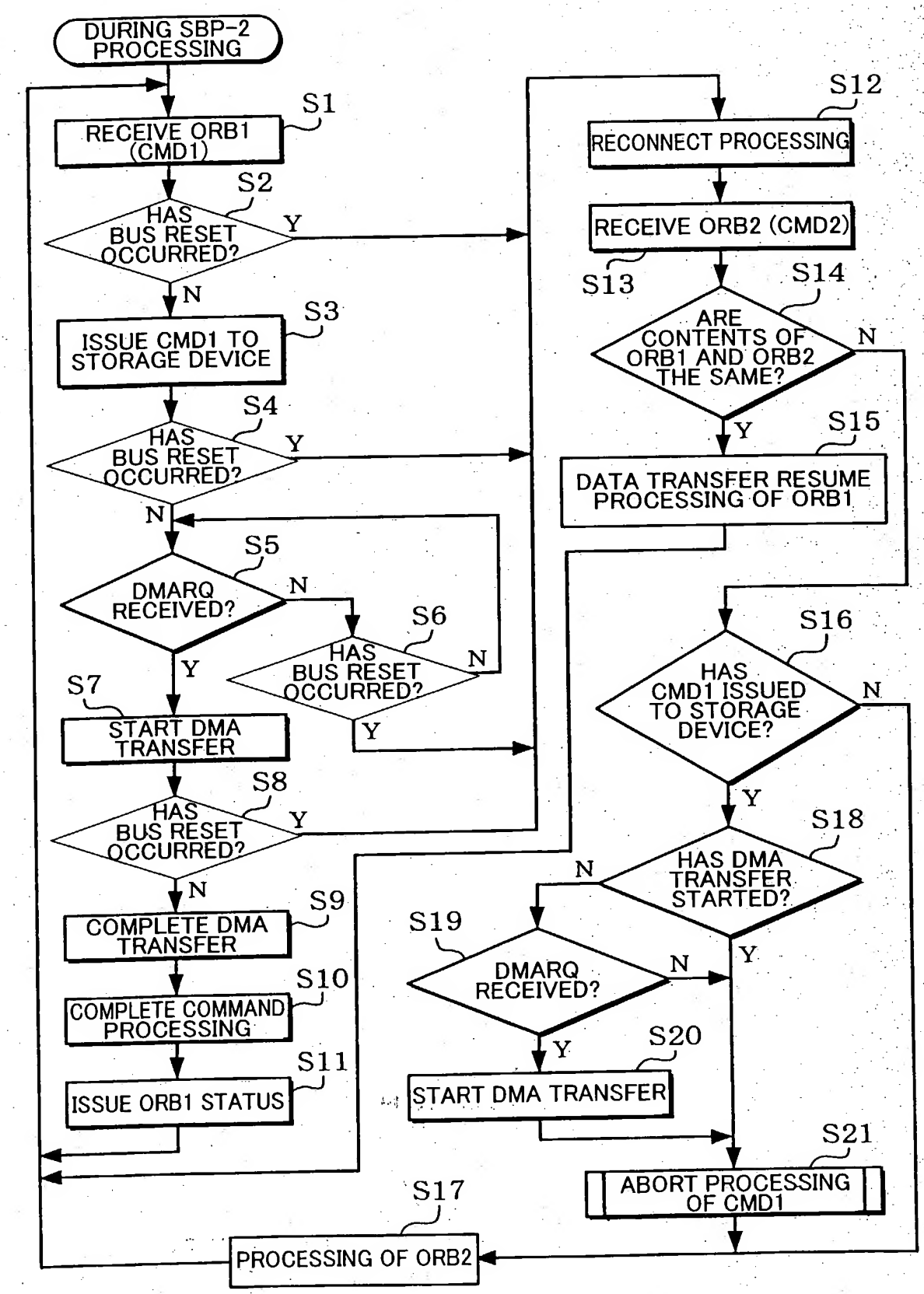
DURING SBP-2 PROCESSING
S1
RECEIVE ORB1 (CMD1)
S2
HAS BUS RESET OCCURRED?
Y
N
S3
ISSUE CMD1 TO STORAGE DEVICE
S4
HAS BUS RESET OCCURRED?
Y
N
S5
DMARQ RECEIVED?
N
Y
S6
HAS BUS RESET OCCURRED?
N
Y
S7
START DMA TRANSFER
S8
HAS BUS RESET OCCURRED?
Y
N
S9
COMPLETE DMA TRANSFER
S10
COMPLETE COMMAND PROCESSING
S11
ISSUE ORB1 STATUS
S12
RECONNECT PROCESSING
RECEIVE ORB2 (CMD2)
S13
S14
ARE CONTENTS OF ORB1 AND ORB2 THE SAME?
N
Y
S15
DATA TRANSFER RESUME PROCESSING OF ORB1
S16
HAS CMD1 ISSUED TO STORAGE DEVICE?
N
Y
S18
HAS DMA TRANSFER STARTED?
N
Y
S19
DMARQ RECEIVED?
N
Y
S20
START DMA TRANSFER
S21
ABORT PROCESSING OF CMD1
S17
PROCESSING OF ORB2

FIG. 10

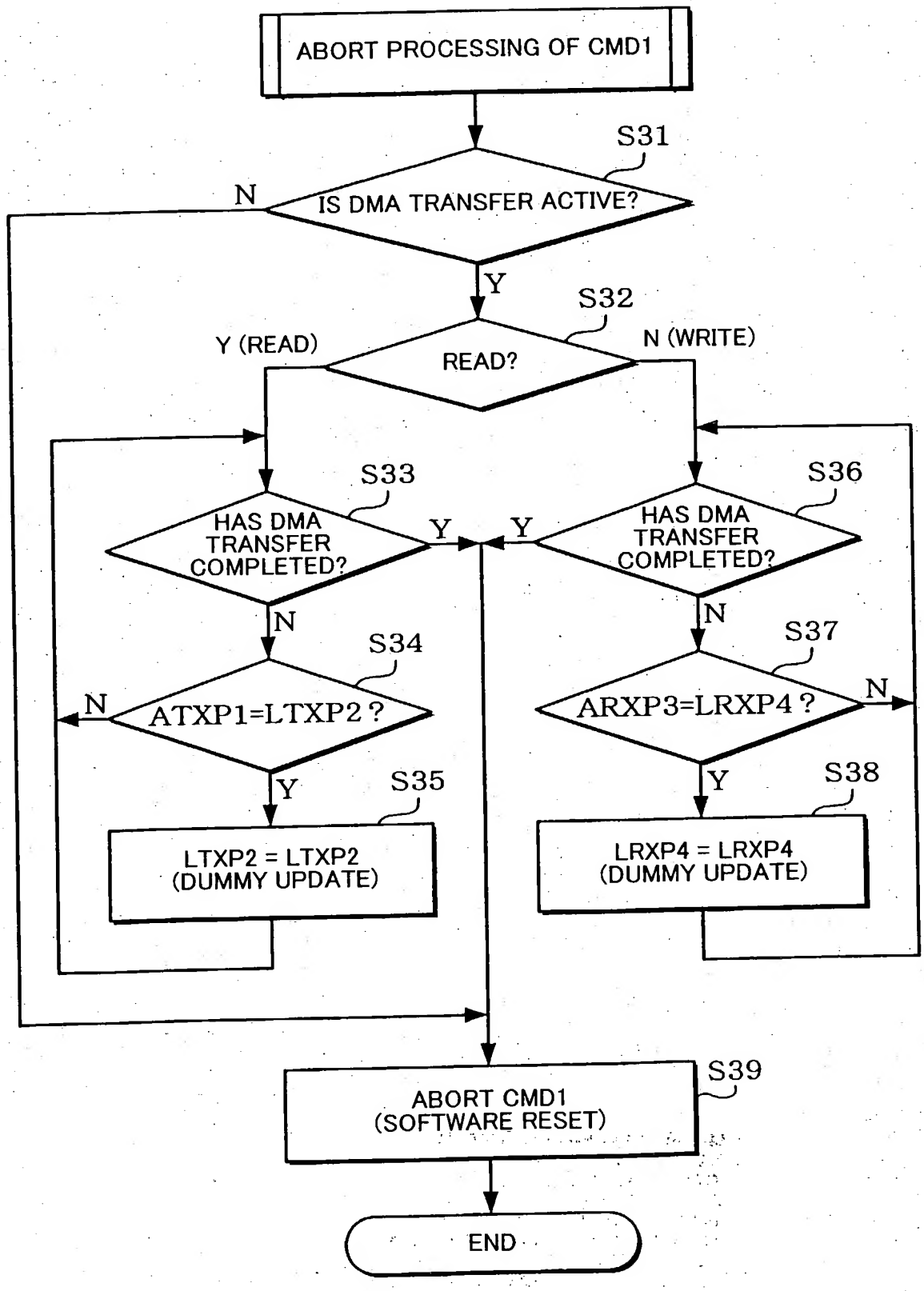
ABORT PROCESSING OF CMD1
S31
IS DMA TRANSFER ACTIVE?
N
Y
S32
READ?
Y (READ)
N (WRITE)
S33
HAS DMA TRANSFER COMPLETED?
Y
N
S34
ATXP1=LTXP2 ?
N
Y
S35
LTXP2 = LTXP2 (DUMMY UPDATE)
S36
HAS DMA TRANSFER COMPLETED?
Y
N
S37
ARXP3=LRXP4 ?
N
Y
S38
LRXP4 = LRXP4 (DUMMY UPDATE)
S39
ABORT CMD1 (SOFTWARE RESET)
END

FIG. 11

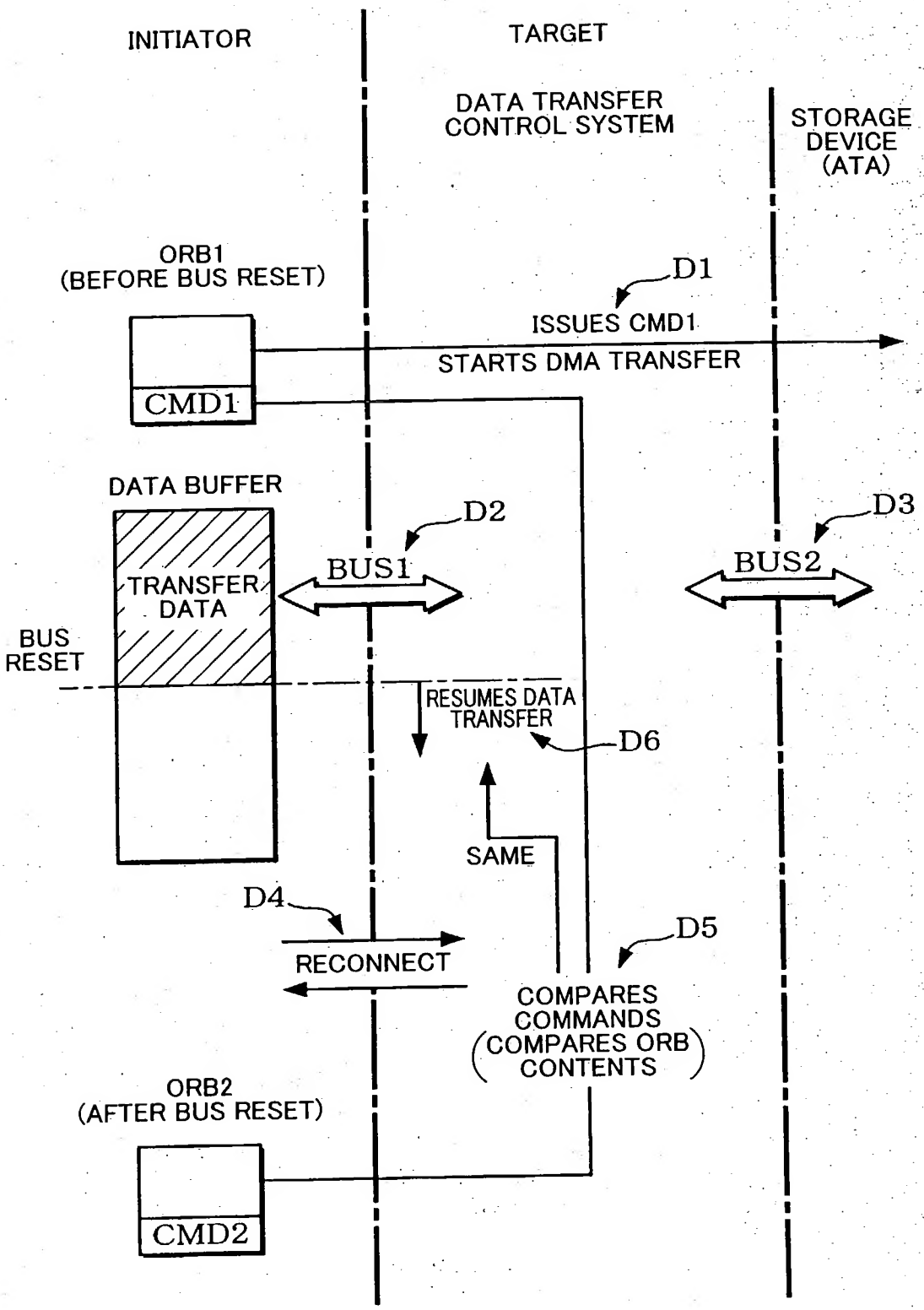
INITIATOR
TARGET
DATA TRANSFER CONTROL SYSTEM
STORAGE DEVICE (ATA)
ORB1 (BEFORE BUS RESET)
D1
ISSUES CMD1
STARTS DMA TRANSFER
CMD1
DATA BUFFER
D2
D3
BUS1
BUS2
TRANSFER DATA
BUS RESET
RESUMES DATA TRANSFER
D6
SAME
D4
D5
RECONNECT
COMPARES COMMANDS (COMPARES ORB CONTENTS)
ORB2 (AFTER BUS RESET)
CMD2

FIG. 12

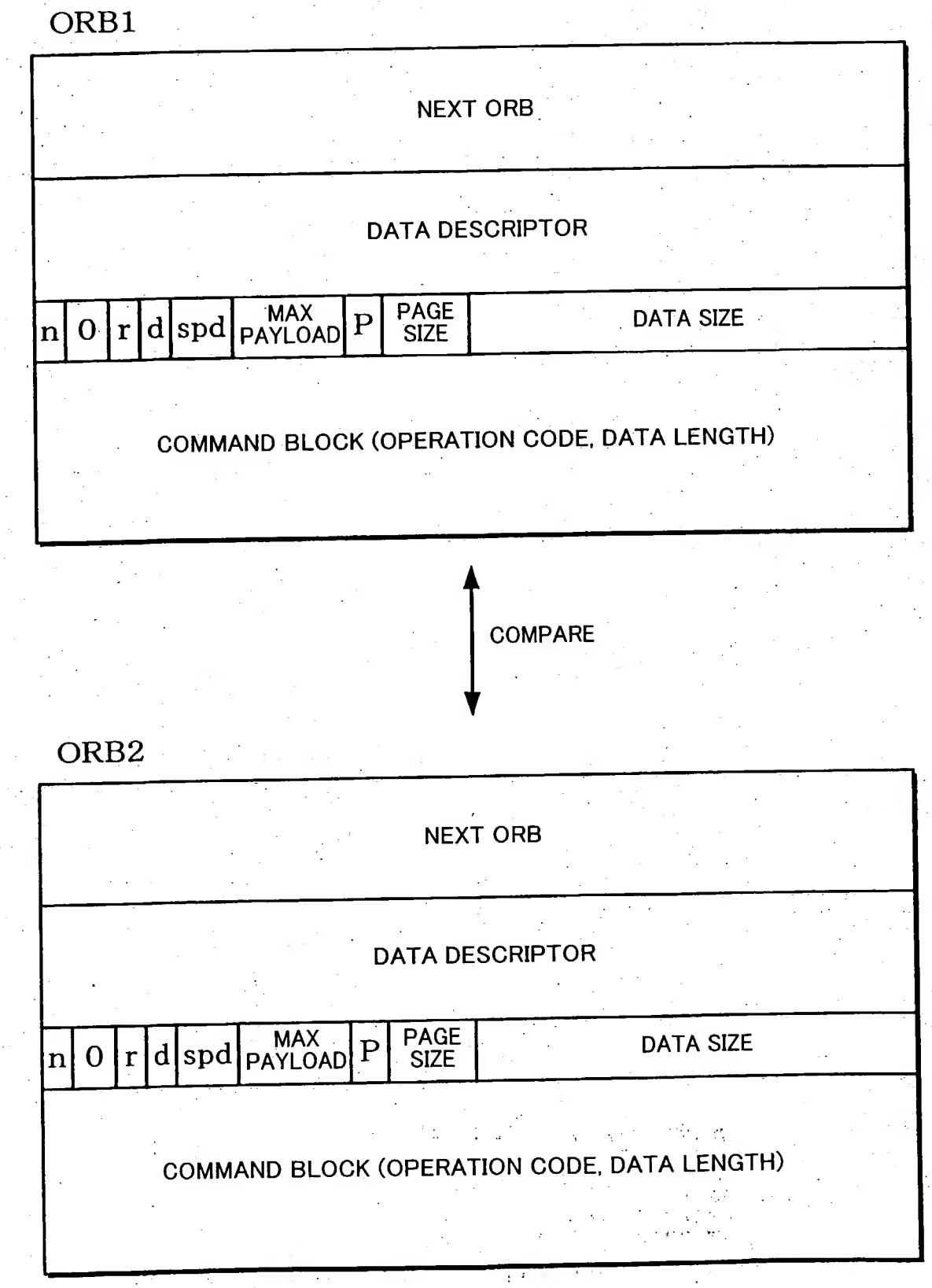
ORB1
NEXT ORB
DATA DESCRIPTOR
n
0
r
d
spd
MAX PAYLOAD
P
PAGE SIZE
DATA SIZE
COMMAND BLOCK (OPERATION CODE, DATA LENGTH)
COMPARE
ORB2
NEXT ORB
DATA DESCRIPTOR
n
0
r
d
spd
MAX PAYLOAD
P
PAGE SIZE
DATA SIZE
COMMAND BLOCK (OPERATION CODE, DATA LENGTH)

FIG. 13

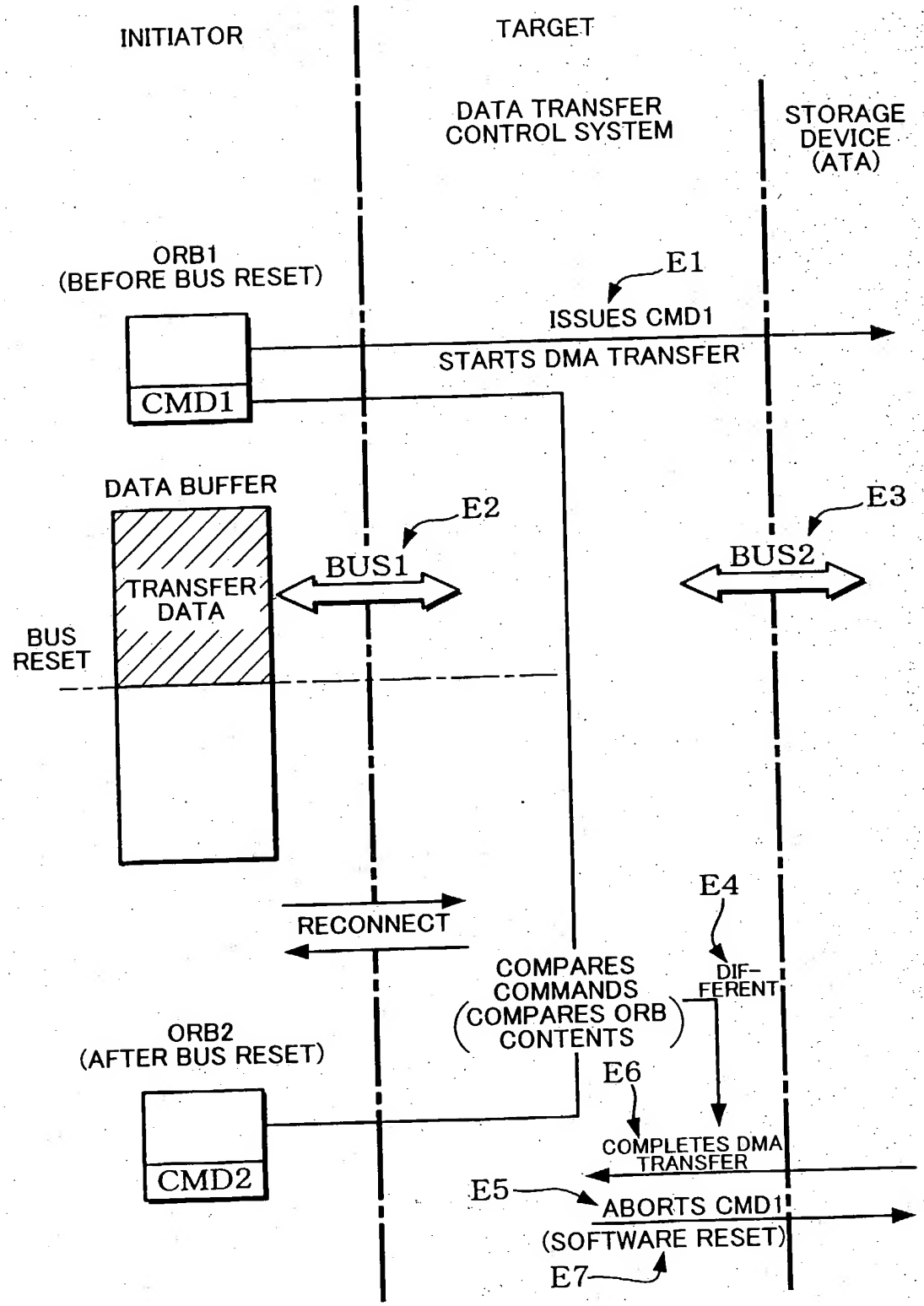
INITIATOR
TARGET
DATA TRANSFER CONTROL SYSTEM
STORAGE DEVICE (ATA)
ORB1 (BEFORE BUS RESET)
E1
ISSUES CMD1
STARTS DMA TRANSFER
CMD1
DATA BUFFER
E2
E3
BUS1
BUS2
TRANSFER DATA
BUS RESET
RECONNECT
E4
COMPARES COMMANDS (COMPARES ORB CONTENTS)
DIF-FERENT
ORB2 (AFTER BUS RESET)
E6
CMD2
COMPLETES DMA TRANSFER
E5
ABORTS CMD1 (SOFTWARE RESET)
E7

FIG. 14A

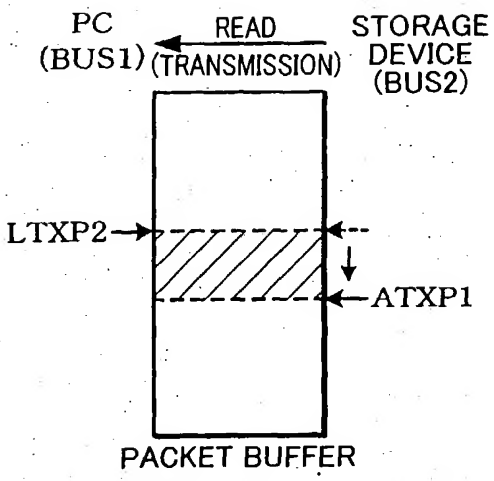

FIG. 14B

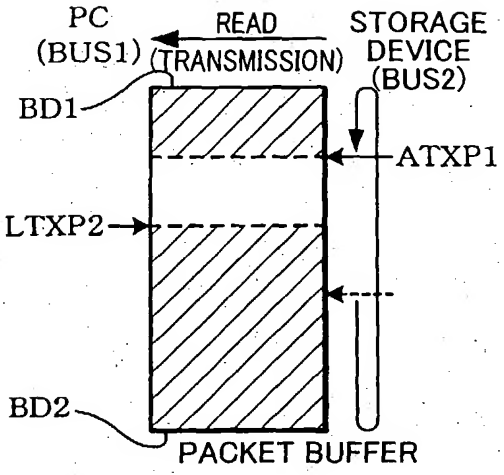

FIG. 14C

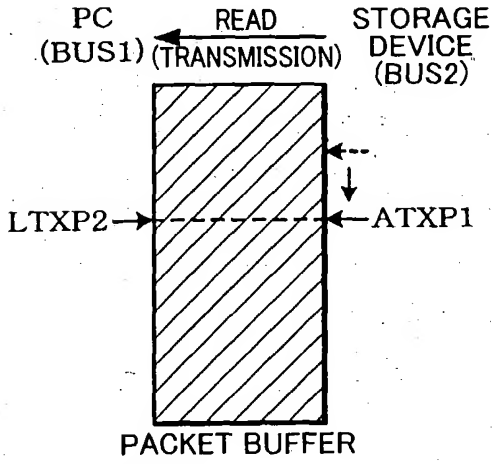

FIG. 14D

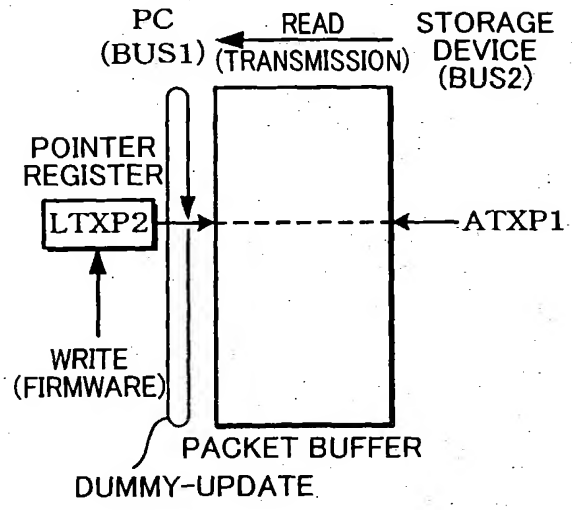

FIG. 14E

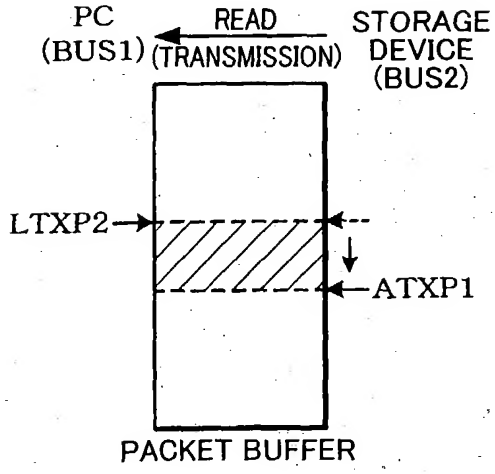

FIG. 15A

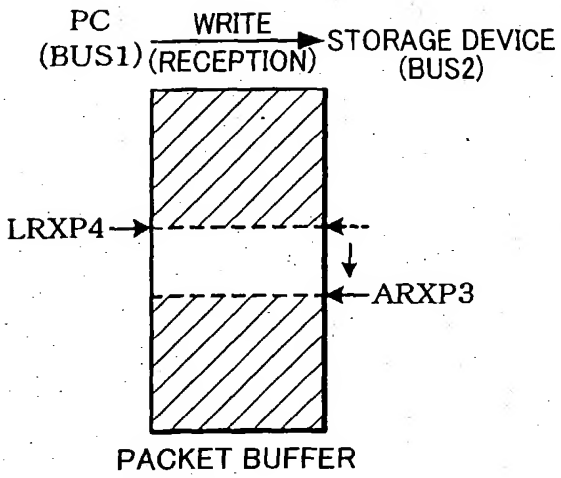

FIG. 15B

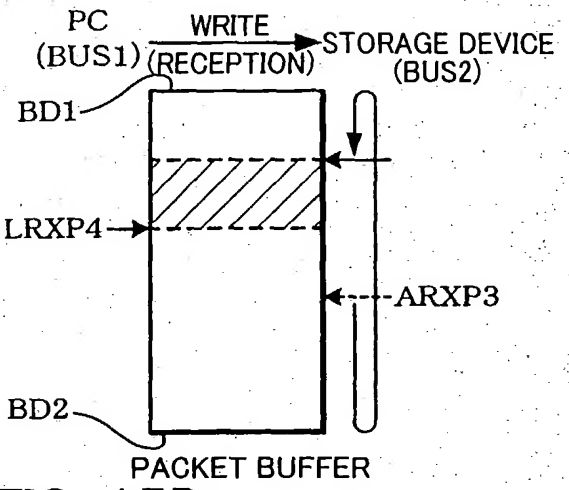

FIG. 15C

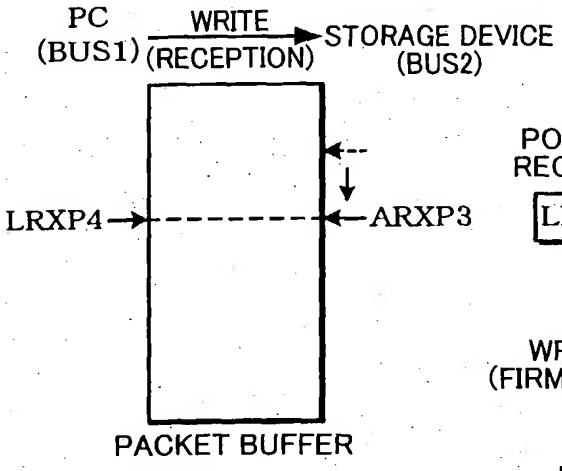

FIG. 15D

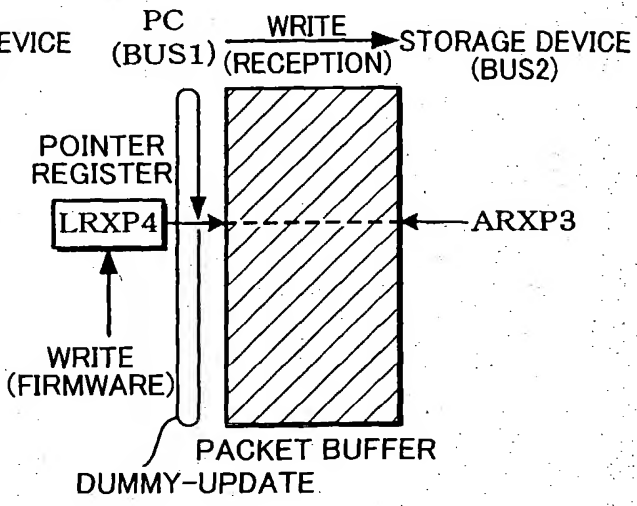

FIG. 15E

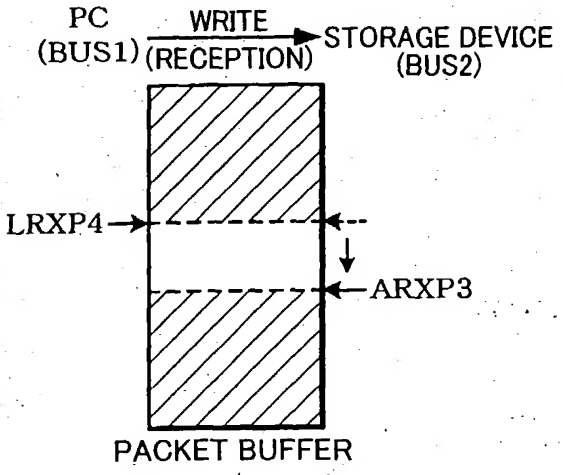

FIG. 16

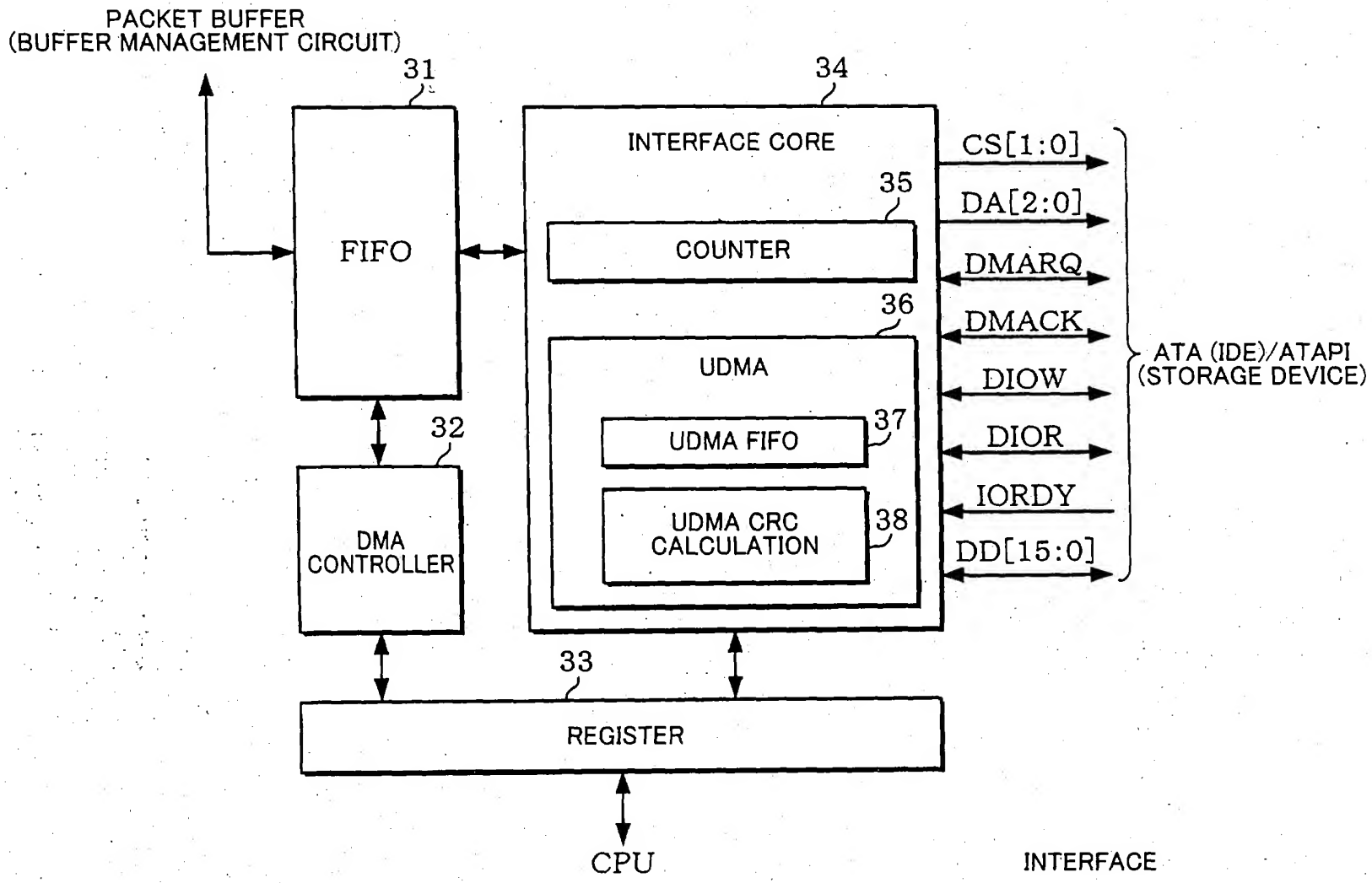
PACKET BUFFER
(BUFFER MANAGEMENT CIRCUIT)
31
34
FIFO
INTERFACE CORE
35
COUNTER
36
UDMA
37
UDMA FIFO
38
UDMA CRC
CALCULATION
32
DMA
CONTROLLER
33
REGISTER
CPU
CS[1:0]
DA[2:0]
DMARQ
DMACK
DIOW
DIOR
IORDY
DD[15:0]
ATA (IDE)/ATAPI
(STORAGE DEVICE)
INTERFACE

FIG. 17A

PIO READ (STORAGE DEVICE → DATA TRANSFER CONTROL SYSTEM → PC)

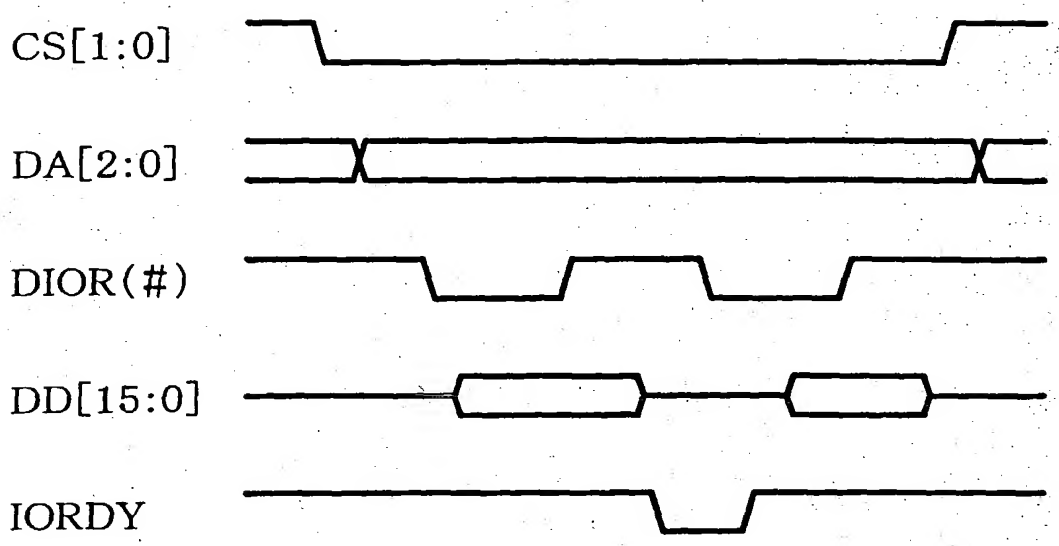

FIG. 17B

PIO WRITE (PC → DATA TRANSFER CONTROL SYSTEM → STORAGE DEVICE)

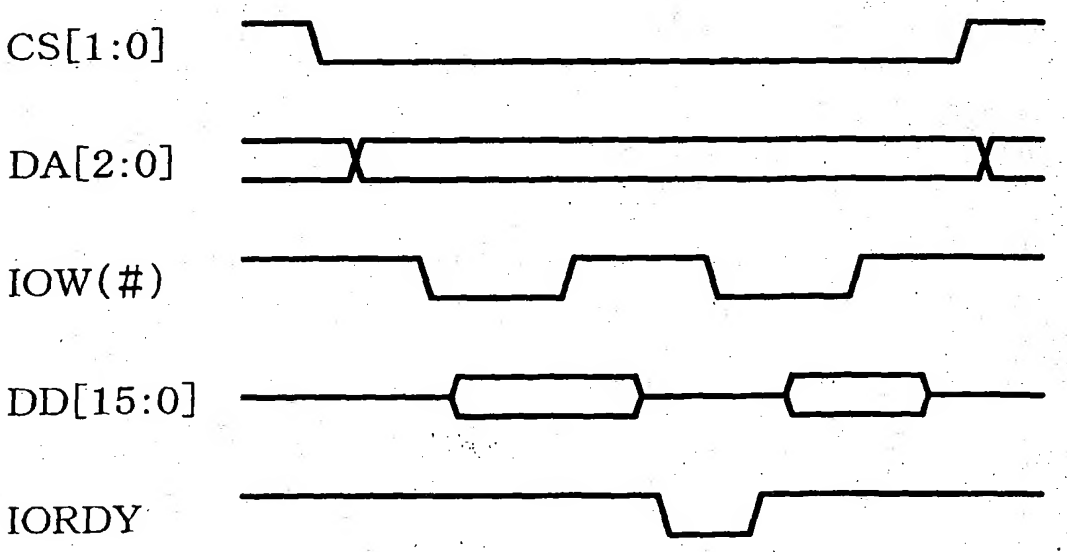

FIG. 18A

DMA READ (STORAGE DEVICE → DATA TRANSFER CONTROL SYSTEM → PC)

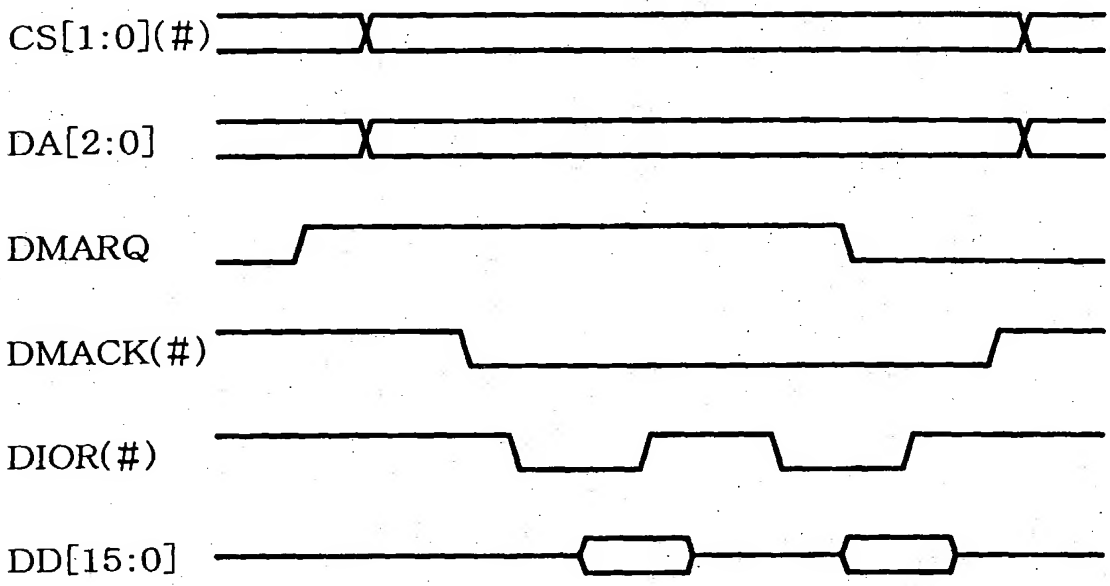

FIG. 18B

DMA WRITE (PC → DATA TRANSFER CONTROL SYSTEM → STORAGE DEVICE)

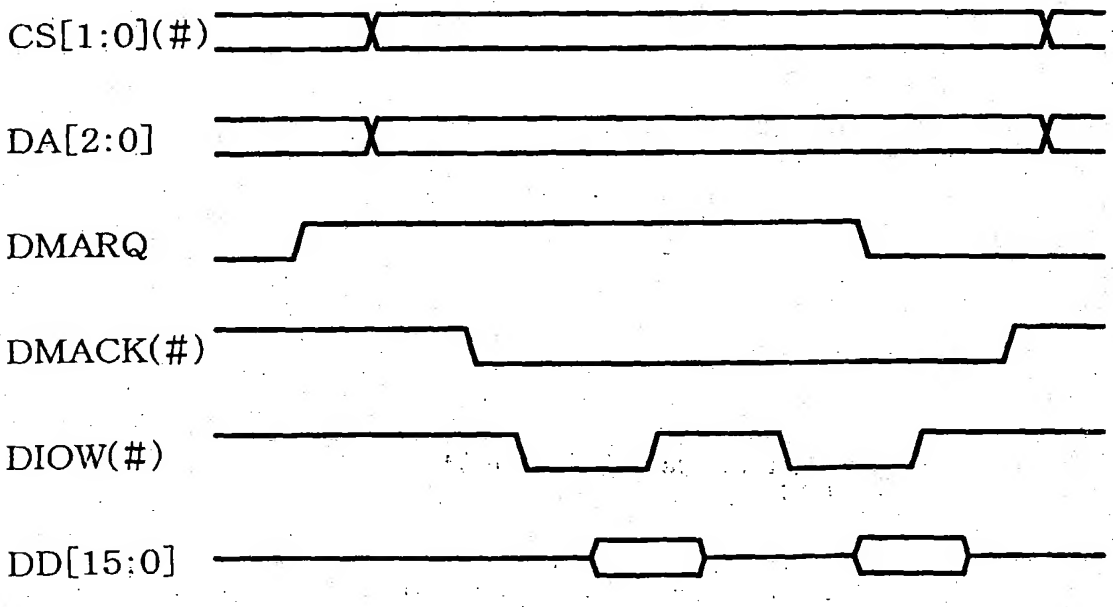

FIG. 19A

UltraDMA READ (STORAGE DEVICE → DATA TRANSFER CONTROL SYSTEM → PC)

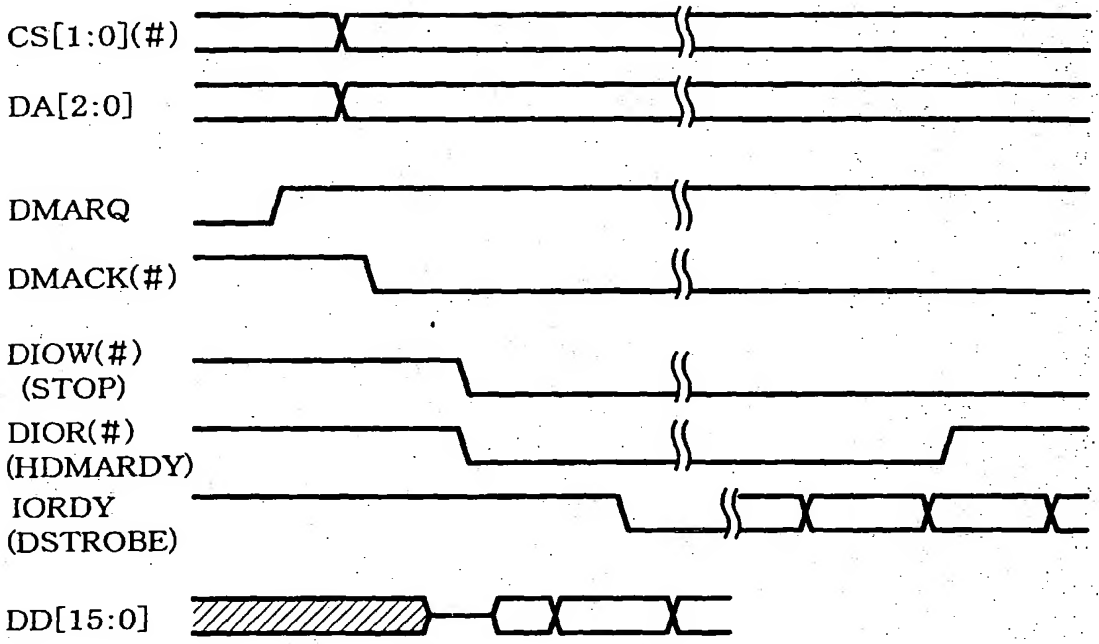

FIG. 19B

UltraDMA WRITE (PC → DATA TRANSFER CONTROL SYSTEM → STORAGE DEVICE)